## REMARKS

Claims 1-18 are pending in the present application. Replacement claims 1, 3, 5, 7, 9, 11, 13, 15, and 17 have been presented herewith.

## Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119 and receipt of the certified copy of the priority document.

## Drawings

The drawings have been objected to under 37 C.F.R. 1.84(p)(5), as including reference numeral 211 in Fig. 2(D) that is not mentioned in the description. Responsive to this objection, the specification has been corrected on page 11 to generally describe formation of a fifth diffusion layer 211 in first diffusion layer 203. Incidentally, fifth diffusion layer 211 may be interpreted as similar to fifth diffusion layer 111 of Fig. 1(F), as described on page 7, lines 14-15 and page 8, lines 16-18. Thus, this correction of the specification should not be construed as new matter. Accordingly, Applicant respectfully submits that the drawings are in compliance with 37 C.F.R. 1.84(p)(5), and respectfully urges the Examiner to withdraw this objection.

## Claim Objections

Claims 1-18 have been objected to for the reasons given on page 2 of the

current Office Action dated November 7, 2002. The claims have been amended as suggested by the Examiner to correct the corresponding informalities. The Examiner is therefore respectfully requested to withdraw this objection.

**Claim Rejections-35 U.S.C. 112**

Claims 1-18 have been rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite. Although Applicant does not concede that the use of "predetermined" in the claims is indefinite since Applicant may describe elements in any manner so long as not to be contradictory of well-known art terminology, the claims have been amended to remove the term "predetermined", to advance prosecution of this application. Applicant respectfully submits that the claims are in compliance with 35 U.S.C. 112, second paragraph, and respectfully urges the Examiner to withdraw this rejection.

**Claim Rejections-35 U.S.C. 102**

Claims 1, 5-7, 11-13, 17 and 18 have been rejected under 35 U.S.C. 102(a) as being anticipated by the Efland et al. reference (U.S. Patent No. 6,137,140). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method of manufacturing an LDMOS transistor of claim 1 includes in combination "implanting ions of the first conductivity type into a part of the well region"

and "forming a gate oxide layer on the surface of the semiconductor substrate, said forming a gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the first conductivity type on the surface of the semiconductor substrate". As further featured, "said implanting ions is carried out with an energy set so that an accelerated oxidation during said forming a gate oxide layer is inhibited". Applicant respectfully submits that the Efland et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has alleged that Fig. 3 of the Efland et al. reference discloses all the features of claim 1. However, the very general description of Fig. 3 in column 4, lines 7-20 does not specifically set forth in detail processing steps. As described beginning in column 4, line 7 of the Efland et al. reference, Fig. 3 illustrates an SCR-LDMOS 30 formed using planar LDMOS fabrication techniques, similar to device 10. The Efland et al. reference as relied upon by the Examiner with respect to Fig. 3, does not specifically describe or even remotely suggest implanting ions into a well region, and subsequently forming a gate oxide thereon, wherein the gate oxide formation includes subjecting the substrate to a heat treatment to diffuse the implanted ions to form a diffusion region. That is, there is no description of how well region 34 is formed, and more particularly how with respect to formation of planar gate oxide layer 39. There is no suggestion in the Efland et al. reference that implanted ions are diffused in well 34 during formation of planar gate oxide layer 39.

Moreover, the Efland et al. reference does not disclose or even remotely suggest implanting ions, prior to gate oxide formation, with an energy set so that an accelerated oxidation during subsequent formation of a gate oxide layer is inhibited. There is no consideration of accelerated oxidation and implant energy in general. Accordingly, Applicant respectfully submits that the method of manufacturing an LDMOS transistor of claim 1 distinguishes over the prior art as relied upon by the Examiner, and that this rejection of claims 1, 5 and 6 is improper for at least these reasons.

Applicant also respectfully submits that the methods of manufacturing an LDMOS transistor of respective independent claims 7 and 13 distinguish over the Efland et al. reference for at least somewhat similar reasons as set forth above. Particularly, the Efland et al. reference does not disclose implanting ions into a well region, then forming a gate oxide layer as including subjecting the semiconductor substrate to a heat treatment to diffuse the implanted ions, whereby implanting of the ions is carried out with an energy so that an accelerated oxidation during forming of the gate oxide layer is inhibited. Accordingly, Applicant respectfully submits that the methods of manufacturing an LDMOS transistor of respective claims 7 and 13 distinguish over the Efland et al. reference as relied upon by the Examiner, and that this rejection of claims 7, 11-13, 17 and 18 is improper for at least these reasons.

## Claim Rejections-35 U.S.C. 103

Claims 2-4, 8-10 and 14-16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Efland et al. reference. Applicant respectfully submits that the Examiner's reliance upon the Efland et al. reference does not overcome the above noted deficiencies. Particularly, the Efland et al. reference does not disclose or even remotely suggest implanting ions into a well, and then forming a gate oxide layer thereon as including a heat treatment to diffuse the implanted ions, wherein the ion implantation is carried out with an energy set so that an accelerated oxidation during forming of the gate oxide layer is inhibited.

## Conclusion

Applicant respectfully submits that claims 3, 5, 9, 11, 15 and 17 have been amended merely to improve form and overcome informalities, rather than to further distinguish over the relied upon prior art. Accordingly, the amendments to these claims should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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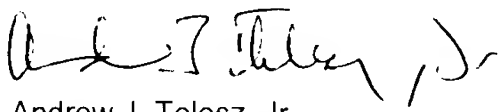

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Enclosures: Version with Marked-Up Changes

## VERSION WITH MARKED-UP CHANGES

**Additions/Deletions to the Abstract:**

A method of manufacturing an LDMOS transistor [comprises] includes providing a semiconductor substrate of a first conductivity type having a well region of a second conductivity type formed on a surface of the substrate. Ions of the first conductivity type are implanted into a part of the well region with a predetermined energy. The substrate is subjected to a heat treatment so that the implanted ions are diffused to form a diffusion region of the first conductivity type on the surface of the substrate. Then, a gate oxide layer and a gate electrode are formed on the surface of the substrate. Finally, a drain region is formed on the surface of the substrate. The predetermined energy for the implantation is set so that an accelerated oxidation during a formation of the gate oxide layer is inhibited.

**Additions/Deletions to the Specification:**

***Page 5, lines 7-16:***

Subsequently, a first insulating film 104 is formed on the semiconductor substrate 101 of the first conductivity type, and a portion [on] of the first insulating film 104 above the first diffusion layer 103 of the second conductivity type is opened (first opening). The first insulating film 104 is formed [in] to a thickness of about 5000 angstroms by a known oxidation technique. [Subsequently, a] A known photolithography/etching technique is used to open the first insulating film 104 in a

region forming a D well, and a first insulating film 104b is formed in about 200 angstroms by the known oxidation technique.

***Page 9, lines 9-19:***

First, a first diffusion layer (well) 203 of the second conductivity type is formed in a portion on a semiconductor substrate 201 of the first conductivity type. Next, a first insulating film 204 is formed on the semiconductor substrate 201 of the first conductivity type. A portion [on] of the first insulating film 204 above the first diffusion layer 203 of the second conductivity type is opened, and a first opening 204a is formed. (Fig. 2(A)) A second diffusion layer (D well) 205 of the first conductivity type is formed in a portion in the first diffusion layer 203 of the second conductivity type via the first opening 204a. (Fig. 2(A))

***Page 11, lines 6-10:***

Subsequently, a fifth diffusion layer 211 in first diffusion layer 203, and a sixth diffusion layer 212 of the first conductivity type is formed in a portion in the second diffusion layer 205 of the first conductivity type and connected to the second diffusion layer 205 of the first conductivity type. (Fig. 2 (D)).

**Additions/Deletions to the Claims:**

1. (Amended) A method of manufacturing an LDMOS transistor comprising:

providing a semiconductor substrate of a first conductivity type having a well region of a second conductivity type formed on a surface thereof;

implanting ions of the first conductivity type into a part of the well region [with a predetermined energy];

forming a gate oxide layer on the surface of the semiconductor substrate,

said forming a gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the first conductivity type on the surface of the semiconductor substrate;

forming [a gate oxide layer and] a gate electrode on the surface of the semiconductor substrate; and

forming a drain region on the surface of the semiconductor substrate,

wherein said implanting ions is carried out with an [the predetermined] energy [is] set so that an accelerated oxidation during said forming a [formation of the] gate oxide layer is inhibited.

3. (Amended) A method of manufacturing an LDMOS transistor according to claim 1, wherein the [predetermined] energy is about 500KeV.

5. (Amended) A method of manufacturing an LDMOS transistor according to claim 1, wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed.

7. (Amended) A method of manufacturing an LDMOS transistor comprising:

providing a semiconductor substrate of a first conductivity type having a first well region of a second conductivity type formed on a surface thereof, and a second well region of the first conductivity type formed within the first well;

implanting ions of the second conductivity type into a part of the second well region [with a predetermined energy];

forming a gate oxide layer on the surface of the semiconductor substrate,

said forming a gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the second conductivity type on the surface of the semiconductor substrate within the second well;

forming [a gate oxide layer and] a gate electrode on the surface of the semiconductor substrate; and

forming a drain region on the surface of the semiconductor substrate,

wherein [the predetermined] said implanting ions is carried out with an energy [is] set so that an accelerated oxidation during said forming a [formation of the] gate oxide layer is inhibited.

9. (Amended) A method of manufacturing an LDMOS transistor according to claim 7, wherein the [predetermined] energy is about 500KeV.

11. (Amended) A method of manufacturing an LDMOS transistor according to

claim 7, wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed.

13. (Amended) A method of manufacturing an LDMOS transistor comprising:

providing a semiconductor substrate of a first conductivity type having a first well of a second conductivity type formed on a surface thereof within a first region, and a second well of the first conductivity type formed within a second region that is inside of the first region;

implanting ions of the second conductivity type into the second well [with a predetermined energy];

forming a gate oxide layer on the surface of the semiconductor substrate,

said forming a gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the second conductivity type located in a third region that is inside of the second region;

forming [a gate oxide layer and] a gate electrode on the surface of the semiconductor substate, the gate oxide layer extending from the first region to the third region through the second region; and

forming a drain region on the surface of the semiconductor substrate within the first region,

wherein said implanting ions is carried out with an [the predetermined] energy [is] set so that an accelerated oxidation during said forming a [formation of the] gate oxide layer is inhibited.

15. (Amended) A method of manufacturing an LDMOS transistor according to claim 13, wherein the [predetermined] energy is about 500KeV.

17. (Amended) A method of manufacturing an LDMOS transistor according to claim 13, wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed.